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Department of Computer Engineering	
Digital Circuit Design I (66221)	
Total Credits	**3**
major compulsory	
Prerequisites	P1 : Computer Programming (66111)

Course Contents

Topics covered includes: Arithmetic system, basic gates, k-map, SOP, POS, ROM, multiplexers, flip-flops, adders, decoders, encoders, synchronous sequential circuits, algorithmic state machine.

	Intended Learning Outcomes (ILO's)	Student Outcomes (SO's)	Contribution
1	Ability to solve problems in binary, octal and hexadecimal system and coding in general and to use Boolean logic and k-maps to minimize Boolean expressions.	A	35 %
2	Knowledge and understanding of digital circuits fundamentals necessary to analyze and design complex digital devices.	C	25 %
3	Design and use major digital combinational components such as multiplexers, decoders, and ROMS, as well as the design and analysis of sequential circuits.	E	40 %

Textbook and/ or Refrences

1. Digital Design , 4th edition By Morris Mano.

Assessment Criteria	Percent (%)
First Exam	20 %
Second Exam	20 %
Homeworks	10 %
Final Exam	50 %

Course Plan

Week	Topic
1-2	Digital Systems and Binary Numbers - Digital Systems - Binary Numbers - Number-Base Conversions - Octal and Hexadecimal Numbers - Complements - Signed Binary Numbers - Binary Codes - Binary Storage and Registers - Binary Logic
3-4	Boolean Algebra and Logic Gates - Basic Definitions - Axiomatic Definition of Boolean Algebra - Basic Theorems and Properties - Boolean Functions - Canonical and Standard Forms - Other Logic Operations - Digital Logic Gates - Integrated Circuits
5-6	Gate-Level Minimization - The Map Method - Four-Variable Map - Five-Variable Map - Production-of-Sums Simplification - Don't-Care Conditions - NAND and NOR Implementation - Other Two-Level Implementation - Exclusive-Or Function
7-9	Combinational Logic - Combinational Circuits - Analysis Procedure - Design Procedure - Binary Adder-Subtractor - Decimal Adder - Binary Multiplier - Magnitude Comparator - Decoders - Encoders - Multiplexers
10-12	Synchronous Sequential Logic - Sequential Circuits - Storage Elements: Latches - Storage Elements: Flip-Flops - Analysis of Clocked Sequential Circuits - State Reduction and Assignment - Design Procedure
13-14	Registers and Counters - Registers - Shift Registers - Ripple Counters - Synchronous Counters - Other Counters
15-16	Memory and Programmable Logic - Random-Access Memory - Memory Decoding - Error

	Detection and Correction - Read-Only memory - Programmable Logic Array - Programmable Array Logic - Sequential Programmable Devices