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Department of Computer Engineering	
Digital Circuit Design II (66321)	
Total Credits	**3**
major compulsory	
Prerequisites	P1 : Digital Circuit Design I (66221)

Course Contents

Algorithmic state machines, analysis and design of asynchronous sequential circuits, programmable logic devices (PLA, PAL, CPLD, FPGA), electrical characteristic of logic gates and the interpretation of datasheets.

	Intended Learning Outcomes (ILO's)	Student Outcomes (SO's)	Contribution
1	Design Digital Systems using Algorithmic State Machine.	E	25 %
2	Design and analyze Asynchronous Digital Circuits	C	20 %
3	Understand the basic concepts of the programmable logic devices (PAL, PLA, CPLD and FPGA) and how to use the hardware description languages such as VHDL in the design, modeling and simulation of digital systems.	C	50 %
4	Demonstrate an understanding of electrical characteristics of logic gates in order to read and interpret datasheets.	A	5 %

Textbook and/ or Refrences

Digital Design 4th edition, by M. Morris Mano. Circuit Design and Simulation with VHDL by Volnei Pedroni. 2nd edition. mit pres. VHDL for Engineers: Pearson New International Edition by Kenneth L. Short

Assessment Criteria	Percent (%)
First Exam	20 %
Second Exam	20 %
Homeworks	10 %
Projects	10 %
Final Exam	40 %

Course Plan

Week	Topic
1	Introduction (Brief review to the basic concepts in the digital design).
2	Programmable Logic devices (Programmable Logic Array (PLA) and Programmable Array Logic (PAL), Complex Programmable Logic Devices (CPLD), Field Programmable Gate Array (FPGA))
3- 5	Algorithmic State Machine (ASM): (ASM chart, Data Processor , Controller design using Flip Flops, Controller design using Decoders and Multiplexers, Controller design using PLDs and ROM)
5	First exam
6- 8	Asynchronous Circuits (Synchronous Vs. Asynchronous, Analysis of Fundamental Mode Circuits, Tabular Representation, Synthesis of Fundamental Mode Circuits, Hazards, Races, Cycles)
9- 14	Hardware Description Languages and Design Tools (Overview of HDL , VHDL overview, Verilog overview, SystemC overview , Design and Analysis Tools)
9- 14	VHDL: (VHDL history, VHDL structural elements, Data types, Operators, Sequential statements, Concurrent statements, RTL style, Hierarchical Model Layout , Simulation and

	Synthesis , Design Examples)
14	Second exam
15-16	Electrical Characteristics of Logic Gates (IC logic families, Electrical characteristics , Noise margin , Propagation delay, DC and AC fan-out)
15-16	Clock Generators and Timing Circuits (Monostable Circuits, Astable Multivibrators, XTAL Clock generators)
16	Final exam