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Department of Computer Engineering	
Computer Architecture I (66323)	
Total Credits	**3**
major compulsory	
Prerequisites	P1 : Microprocessors (66322)

Course Contents

Topics include Performance evaluation, instruction set computer architectures (RISC), ALU design and Control Unit design using the MIPS central processor as an example.

	Intended Learning Outcomes (ILO's)	Student Outcomes (SO's)	Contribution
1	Gain knowledge and necessary skills to compare different computer system organizations and designs and be able analyze and compare performances of different architectures and implementations.	E	15 %
2	Have understanding of the MIPS ISA design and implementations.	J	35 %
3	Acquire skills in the design and implementation of the Datapath (Registers, ALU), Control (single cycle, multi-cycle, pipelining) and a Cache design of the MIPS processor and other RISC processors.	C	50 %

Textbook and/ or Refrences

Computer Organization and Design: The Hardware/Software Interface 4th edition. Authors David Patterson and John Hennessy.

Assessment Criteria	Percent (%)
First Exam	22 %
Second Exam	22 %
Homeworks	6 %
Final Exam	50 %

Course Plan

Week	Topic
1	Coursed Overview and introduction
2	Comparison of different architectures
3	MIPS Instructions format and instruction set
4	MIPS instructions continue
5	Midterm Exam I
6	Performance evaluation
7	ALU design: 1- bit and 32 bit ALU
8	ALU add/subtract and multiply units operations
9	Single and multicycledatapath
10	Midterm Exam 2
11	Multicycle control design and implementation
12	Pipeline design
13	Pipelining hazards
14	Memory Cache design
15	Cache examples
16	Final Exam