0

Department of Computer Engineering	
Very Large Scale Integration (VLSI) (66568)	
Total Credits	**3**
major elective	
Prerequisites	P1 : Computer Architecture I (66323)

Course Contents

1. CMOS logic The Inverter. NAND and NOR gates. Complex Gates Pass Transistors and Transmission Gates. Tristate Logic. Multiplexers. Latches and Flip Flops. 2. CMOS Fabrication and Layout Inverter Cross Section. Fabrication Process: Masks. N-Diffusion, P-Diffusion, Poly-silicon, Wells, and Metal Layers. Layout Design Rules Inverter Layout. NAND, NOR Layout. Standard Cells. Stick Diagrams. 3. MOS Transistor Theory. I-V characteristics. VTC characteristics for an Inverter. Body and non-ideal characteristics. The Capacitance Model. Delay Model. Spice Simulation 4. Performance Evaluation (Delay Estimation). The RC model Analysis Using SPICE. Logical Effort Parasitic Capacitance. Delay in Logic Gates. Multi-Stage Delay. 5. CMOS families Complementary CMOS. Pseudo-NMOS Dynamic Gates. Domino CMOS. Dual Rail Domino Other CMOS families. Silicon over Insulator Circuits (SOI). 6. Sequential Circuit Design. Sequencing and Pipelining. Dynamic CMOS Latches Dynamic CMOS Flip-Flops. Static CMOS latches and Flip-Flops Timing Analysis of Latches and Flip-Flops. 7. Data-path Subsystems 1:Adders (Layout Level) One-bit Adders Carry Ripple Adders Carry Select and Carry Skip Adders Carry look Ahead Adders Other Adders. 8. Data-path Subsystems 2. Comparators Shifters. Counters. Multiplication. 9. Array Logic and Memory Decoders. PALs and PLAs SRAM DRAM 10. Input and Output Pads Pad Input pad Output pad. Bidirectional Pads.

	Intended Learning Outcomes (ILO's)	Student Outcomes (SO's)	Contribution
1	1. Acquire knowledge in CMOS VLSI Circuit Analysis: Area Estimation, Delay Estimation. Analysis of Combinational and Sequential Circuits	C	25 %
2	Acquire knowledge in CMOS VLSI design and implementation at the circuit and Layout Level	C	25 %
3	Acquire the Ability to use VLSI design Tools to analyze, simulate and design VLSI ICs at the Layout Level	K	25 %
4	The Ability to apply the Knowledge of Computer Architecture, Hardwareand VHDL in designing a digital Circuit (IC) at the Layout Level.	E	25 %

Textbook and/ or Refrences

Text Book: Neil Weste and David Harris, CMOS VLSI Design A circuit and Systems Perspective.Addison Wesley

Assessment Criteria	Percent (%)
First Exam	20 %
Second Exam	20 %
Homeworks	15 %
Final Exam	45 %

Course Plan

Week	Topic
1	CMOS logic: Inverter,NAND and NOR gates. Complex Gates Transmission Gates.Latches

	and Flip Flops
2	CMOS Fabrication and Layout:Inverter Cross Section.Fabrication Process: Masks.N-Diffusion, P- Diffusion, Poly-silicon, Wells, and Metal Layers.
3	Layout Design Rules, Inverter Layout. NAND, NOR Layout. Standard Cells Stick Diagrams
4	MOS Transistor Theory: I-V characteristics.VTC characteristics for an Inverter.Delay Model. Spice Simulation
5	Delay Estimation: The RC model. Analysis Using SPICE. Logical Effort. Multi-Stage Delay.
6	CMOS families: Complementary CMOS. Pseudo-NMOS. Domino CMOS. Dual Rail and Others
7	First Exam
8	Sequential Circuit Design. Sequencing and Pipelining. Latches and Flip-Flops
9	Data-path Subsystems 1:Adders One-bit Adders: Carry Ripple Adders: Carry Select and Carry Skip Adders
10	Data-path Subsystems 2:Adders (Layout Level) Fast Adders Carry look Ahead Adders and other FastAdders
11	Data-path Design: Comparators and Shifters.
12	Data-Path Design: Multipliers, Booth Multipliers
13	Array Logic: Decoders. PALs and PLAs.
14	Second Exam
15	Memory: SRAM, EEPROM, Flash DRAM
16	Input and Output Pads
16	Final Exam